

**AMENDMENTS TO THE CLAIMS**

This listing of claims replaces all prior versions and listings of claims in the application:

**Listing of Claims**

1. – 13. (Canceled)

14. (Previously Presented) A computer system, comprising:

a host processor;

a shadow processor coupled to the host processor, the shadow processor adapted to control interrupts received from peripherals connected to a computer processor system;

the host processor in communication with an external bus via an external bus interface, the external bus adapted to transfer data to and from a main processor and at least one memory device;

a memory controller within the host processor for controlling data access to the at least one memory device;

an execution unit for controlling the memory controller and a main processor;

an arithmetic logic unit and a plurality of registers within the host processor;

the memory controller, arithmetic logic unit and registers and host processor being inter-communication via at least one internal bus;

the host processor adapted to process a first set of instructions;

the shadow processor adapted to process a second set of instructions, the second set of instructions being a subset of the first set of instructions; and

the shadow processor adapted to receive control signals and to process instructions in dependence upon those control signals independently of the host processor means.

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